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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,165	09/18/2003	J. Young J. Paik	007734	6290
	7590	10/03/2005	FPS/MMCS/APC/DV	
Patent Counsel, MS/2061 Legal Affairs Department Applied Materials, Inc. P.O. Box 450A Santa Clara, CA 95052			EXAMINER MACARTHUR, SYLVIA	
			ART UNIT	PAPER NUMBER
			1763	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/665,165

Applicant(s)

PAIK, J. YOUNG J.

Examiner

Sylvia R. MacArthur

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>10/8/04 12/7/04</u> . | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1,2,4, 6,10, 12, 13, 15,17, 19, 23-26, 29, and 30 are rejected under 35 U.S.C.

103(a) as being unpatentable over Campbell et al (US 6,350,179) in view of Holzapfel et al WO 98/05066).

Campbell et al teaches a method for determining a polishing recipe based upon the measured pre-polished thickness of a process layer.

Regarding claim 1: Campbell et al teaches a computer-implemented method for updating a process recipe in a CMP process for a wafer comprising the steps of:

- (a) inputting a model for CMP processing of a wafer having at least first and second layers comprising at least one control parameter, said model comprising a first component that predicts a value for a characteristic (film thickness) of the first layer and a second component that predicts a value for a characteristic of the second layer;
- (b) determining a process recipe based upon the model of step (a);
- (c) receiving a measured value of the characteristic of the first layer and/or the characteristic of the second layer for a wafer processed according to the process recipe of step

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(b); and

(d) determining an updated model based upon the difference between the measured value and the predicted value of the characteristic.

Campbell et al teaches a recipe per layer per wafer. See cols 4-6 and Fig. 5

Campbell fails to teach a wafer with a plurality of layers that is polished and the thickness of each layer on that wafer polished and detected.

Holzapfel et al teaches a method and apparatus for the in-process detection and measurement of thin film layers. Wafer 400 has first layer 402 and second layer 404. The motivation to modify the controller of Holzapfel et al to use the process recipes of Campbell et al is that it provides the means to measure and control the thickness of the layers of a wafer. Thus, it would have been obvious for one of ordinary skill in the art at the time of the claimed invention to use the algorithm of Campbell et al with the wafer of Holzapfel et al as the substrate.

Regarding claim 2: The method of claim 1, wherein the model of Campbell et al determines a first process recipe for the first layer of the wafer and a second process recipe for the second layer of the wafer, see Fig. 5.

Regarding claim 4: The method of claim 1, wherein the characteristic of the first and second layers of the

wafer comprises film thickness, and/or the control parameter comprises polishing time, the characteristic discuss in Campbell et al is film thickness, see abstract and in Holzapfel et al is thickness and time, see page 9 lines 11-31.

Regarding claim 6: The method of claim 1, wherein the processing recipe comprises a plurality of polishing steps, see Campbell et al col. 6 lines 34-37.

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Regarding claims 10 and 23: A method (or apparatus) of controlling a characteristic of a wafer in a CMP operation, comprising the steps of:

- (a) providing a model for CMP processing of a wafer having at least first and second layers comprising at least one control parameter capable of being controlled, comprising a first component that predicts a value for a characteristic of the first layer and a second component that predicts a value for a characteristic of the second layer;
- (b) polishing a wafer using a first polishing recipe based upon the model of step (a);
- (c) measuring the wafer characteristic for a wafer processed according to the process recipe of step (b); and
- (d) determining an updated model based upon the difference between the measured value and the predicted value of the wafer characteristic, see col. 6 lines 4-21 and 50-57.

Regarding claims 12 and 24. The method of claim 10, wherein the model determines a first process recipe for the first layer of the wafer and a second process recipe for the second layer of the wafer, see Fig. 5 of Campbell et al.

Regarding claim 15: The method of claim 10, wherein the characteristic of the first and second layers of the wafer comprises film thickness, and/or the control parameter comprises polishing time discuss in Campbell et al is film thickness, see abstract and in Holzapfel et al is thickness and time, see page 9 lines 11-31.

Regarding claims 17 and 28: The polishing process comprises a plurality of polishing steps see Campbell et al col. 6 lines 34-37.

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Regarding claims 19, 26, and 29: The polishing of step (b) comprises polishing the wafer at a plurality of polishing stations, see col. 3 line 58 of Campbell et al

Regarding claim 30: An system for polishing a wafer in a CMP operation having controlled characteristics,

comprising:

(a) a model for comprising at least one control parameter capable of being controlled for CMP processing of a wafer having at least first and second layers, comprising a first component that predicts a value for a characteristic of the first layer and a second component that predicts a value for a characteristic of the second layer;

(b) CMP polishing station for polishing a wafer using a first polishing recipe based upon the model of step (a);

(c) a metrology tool 32 of Campbell et al for measuring the wafer characteristic for a wafer processed according to the process recipe of step (b); and

(d) a computer see col.6 lines 58-67 for calculating an updated model based upon the difference between the measured value and the predicted value of the wafer characteristic.

Campbell et al teaches a method for determining a polishing recipe based upon the measured pre-polished thickness of a process layer.

Campbell et al teaches a recipe per layer per wafer. See cols 4-6 and Fig.5

Campbell fails to teach a wafer with a plurality of layers that is polished and the thickness of each layer on that wafer polished and detected.

Holzapfel et al teaches a method and apparatus for the in-process detection and measurement of thin film layers. Wafer 400 has first layer 402 and second layer 404. The motivation to modify

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the controller of Holzapfel et al to use the process recipes of Campbell et al is that it provides the means to measure and control the thickness of the layers of a wafer. Thus, it would have been obvious for one of ordinary skill in the art at the time of the claimed invention to use the algorithm of Campbell et al with the wafer of Holzapfel et al as the substrate.

3. Claims 3,5,7-9, 11, 14, 16, 18, 20-22, 27, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Campbell et al in view of Holzapfel et al as applied to claims 1,2,4, 6,10, 12, 13, 15,17, 19, 23-26, 29, and 30 above, and further in view of Campbell et al (US 6,230,069 also known as Campbell et al '069).

The teachings of Campbell et al and Holzapfel et al were discussed above.

Neither teaches a specific model for the wafer characteristics.

Campbell et al teaches system and method for controlling a CMP polishing tool, see abstract.

Regarding claims 3 and 14. The model is defined as:

$$Y_t = Y_A + Y_s,$$

where

Y_t is the model for a CMP process for a multi-layer wafer;

Y_A is the model for a CMP process for the first layer of the wafer; and

Y_B is the model for a CMP process for the second layer of the wafer.

This a short hand version of equation 13 of Campbell et al US 6,230,069)

Regarding claims 5, 16,18, and 27: The method of claim 1, wherein the model of step (a) defines a plurality of regions on a

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wafer and a measured value for the wafer characteristic for each of the plurality of regions is received in step , (c), the values a, b of equation 7 take into account the topography of the wafer according to col. 5 lines 20-25 of Campbell et al '069.

Regarding claim 7: The method of claim 1, wherein the model accounts for a tool state of a tool used in the

CMP processing of a wafer, see col. 2 lines 55-67

Regarding claim 8: The method of claim 1, further comprising developing a model, said model development

comprising the steps of

(e) inputting pre-polished wafer characteristics for one or more wafers;

(f) receiving measured values of the wafer characteristics for the one or more wafers processed according to a processing recipe;

(g) providing a model defining the effect of tool state on polishing effectiveness; and

(h) recording the pre-polished and post-polished wafer characteristic on a recordable medium, see col.4 lines 22-46 of Campbell et al '069.

Regarding claim 9: The method of claim 8, wherein model development further comprises fitting the data to a curve that establishes a relationship between the wafer characteristic and the control parameter, see col.7 lines 10-19 of Campbell et al '069.

Regarding claims 11 and 20: The method of claim 10, further comprising:

determining an updated process recipe based upon the updated model of step (d) see col.6 lines 24-60 of Campbell et al '069.

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Regarding claims 13, 21, and 25: The method of claim 10, wherein the model accounts for the tool state of a tool used in the CMP processing of a wafer, see abstract of Campbell et al '069.

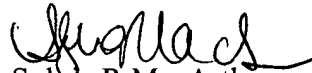
Regarding claim 22: The method of claim 19, wherein, the initial wafer thickness for each of the polishing stations is provided by the prediction from previous polishing stations, factor a considers tool shift, see col. 5 lines 7-19 of Campbell et al '069.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sylvia R. MacArthur whose telephone number is 571-272-1438. The examiner can normally be reached on M-F during the core hours of 9 a.m. and 3 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on 571-272-1435. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Sylvia R MacArthur
Patent Examiner
Art Unit 1763

September 29, 2005